REMARKS

Claims 1 - 38 remain active in this application. The indication of allowability of claims 7 and 9 and the application of prior art only to claims 1 - 6, 8, 35, 36 and 38 is noted with appreciation. The Examiner has indicated that claims 10 - 18 have been withdrawn from consideration as being non-elected, with traverse, in response to a requirement for election of species. The specification has been reviewed and editorial revisions made where seen to be appropriate. Claims 1, 19, 33, 34 and 37 have been amended. New dependent claims 39 - 44 have been added to more fully recite subject matter regarded as the invention. Support for these new claims appears in Figures 9A - 12B and descriptions thereof on pages 18 0 19 of the specification. Amendments of claims 34 and 37 are directed to matters of form. Support for the amendments of claims 1, 19 and 33 is found throughout the application, for example, in Figures 1C - 8B and 10A - 12B and the description thereof, for example, on [page 7, line 31, and page 9, line 22] and on pages 19 - 21. The amendments to the drawings are respectfully submitted to be well-supported by the respective descriptions thereof or self-evident corrections. No new matter has been introduced into the application.

The Examiner's modification of the requirement for election of species resulting in the withdrawal from consideration of only claims 10 - 18 is noted with appreciation. However, the traverse of the requirement is respectfully maintained and further reconsideration is respectfully requested. Again, it is respectfully submitted that different embodiments of both emitter controlled thyristors (ECT) and emitter turn-off (ETO) thyristors and structures for packaging are disclosed as a "*family*" of ECT and ETO) devices which are based on the same operation principle of emitter control

(although different circuits, configurations, packaging and electrical elements may be used to carry out or exploit that principle of operation and which are not equivalents or unpatentable over each other). See page 2, lines 18 - 26. Further, ECT devices and ETO devices are electrically similar and the terminology (e.g. ECT or ETO) is principally used to indicate whether the device is formed monolithically (ECT) or as a hybrid device (ETO) which may include different configurations formed on a single substrate by, for example, stacking as illustrated in Figure 15A, while, as packaged, both are three-terminal devices having generally similar electrical characteristics. Moreover, ETO and ECT devices differ from gate turn-off (GTO) devices by transistor control by switches (which are not limited to transistors by may include diodes, zener diodes and other types of devices) at the emitter (and possibly with additional arrangements for draining or sinking current from the upper base of the thyristor - see Figure 9 and page 18, lines 9 - 18, which may or may not be embodied as switches). Thus ETO thyristors and ECTs are electrically inclusive of elements which could otherwise function as GTOs (which, in accordance with terminology accepted in the art, is a four layer thyristor semiconductor device as packaged or configured.)

Therefore, it is respectfully submitted that neither distinctions between the number and types of transistors or other devices included (e.g. with a GTO) in an ETO thyristor, particularly as packaged, nor a distinction based on the formation thereof as a monolithic or hybrid device is a proper substantive basis for a requirement for election of species or adherence thereto. Moreover, since the species of Figure 17 (which is the preferred embodiment of Figures 17A and 17B) was provisionally elected, Figures 17B and 17C illustrating a GTO/thyristor with two *switches*, Q1

and Q2, limitation of consideration to embodiments "controlled by two MOSFETs" is not in accordance with the election provisionally made. It is also respectfully submitted that such a requirement and limitation on consideration without a strong substantive basis is prejudicial to Applicant in artificially denying consideration of the invention as a *family* of devices operating on a common principle. For example, it is not at all evident that any serious burden would exist in consideration of ETO embodiments and packages (claims 10 - 18) beyond consideration of claims to ECTs (claims 1 - 9 and 33 - 38) and GTO packages, including configurations of the semiconductor structure (claims 19 - 32) and elements forming an ETO thyristor (or ECT) when in combination with a GTO. Accordingly, further reconsideration and withdrawal of the requirement for election of species followed by examination of all claims is respectfully requested.

not OK

The Examiner observes that the application does not include and Abstract and make a requirement therefor. This requirement is respectfully traversed since an Abstract on a separate page 31 was, in fact, included with the original application papers and a copy of that page is attached hereto. Accordingly, provision of a copy of the Abstract page as originally filed is respectfully submitted to be a full and complete response to the Examiner's requirement.

OK

The Examiner has objected to the disclosure and made several specific criticisms. This objection is respectfully traversed, particularly as being either in error or moot in view of the above amendments or concurrently filed Request for Approval of Drawing Revisions. Specifically, all of the Examiner's criticisms appear to be matters of correspondence between the specification and the drawings which, upon approval of the requested revisions of the drawings by the Examiner, are believed to properly correspond. In

regard to notations Q_E and Q_G on page 5, it is respectfully submitted that these notations are not, in fact, reference numerals, particularly with reference to Figures 18 and/or 19 but have, nevertheless, been supplied in those Figures. The reference numeral "74" and legend "P-base" do, in fact, appear in Figure 3A. Other changes in the drawings or the specification are believed self-explanatory. Accordingly reconsideration and withdrawal of this objection to the disclosure is respectfully requested.

Claims 19 - 32 and claims 33 - 38 have been separately rejected under 35 U.S.C. §112, first paragraph, as being non-enabling and failing to reasonably convey possession of the invention as of the filing date, respectively. These rejections are respectfully traversed. In regard to the noted recitations of claim 19 and 23, the noted recitations are well-illustrated in Figures 17A - 17C and the
OK recited connections are well-described at pages 20 - 22. In particular regard to the noted recitations of claim 23, it is respectfully called to the Examiner's attention that, as claimed in claims 23+, each of the first and second switches is constituted by a plurality of parallel-connected devices and the Examiner's
OK paraphrase of the claim recitations is substantively incorrect. In regard to the recitations of claim 33,
OK the superfluous reference to "control electrodes" has been deleted. Therefore, it is respectfully submitted that these rejection are in error or moot in view of the above amendments and reconsideration and withdrawal thereof is respectfully requested.

Claims 19 - 22, 34 and 37 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite; the Examiner stating specific criticisms of claims 19, 34 and 37. This rejection is also respectfully traversed, particularly as being moot in view of the amendments thereto made above. Initially, it is noted

that while the Examiner's criticisms stated in support of this rejection are well-taken, they do not support rejection of the claims since they do not engender ambiguity or obscure the intended scope of the claims. Nevertheless, the criticized language has been amended in direct response to the stated criticisms which are respectfully submitted to be no longer applicable. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

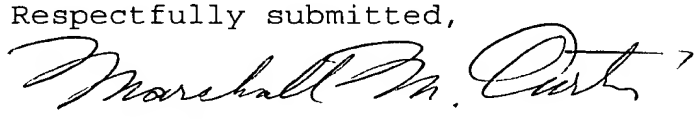
Claims 1 - 6 and 8, insofar as in compliance with 35 U.S.C. §112, have been rejected under 35 U.S.C. §102 as being anticipated by Schlangenotto and claims 35, 36 and 38 have been rejected under 35 U.S.C. §103 as being unpatentable over Schlangenotto. These rejections are also respectfully traversed as being moot in view of the amendments to claims 1 and 33 respectively which have been made above.

Schangenotto is directed to a monolithic ECT structure which, while similar to the embodiment of Figures 1A and 1B of the present invention, does not teach or suggest particular features of configuration or packaging or additional electrical elements of other embodiments now claimed in claims 1 and 33 (and claim 19) in a manner generic to all other disclosed embodiments of the invention. Therefore, it is respectfully submitted that Schlangenotto cannot anticipate or support a conclusion of obviousness of any claim in the application since claims 1 and 33 and claims depending therefrom have been clearly distinguished therefrom by features of circuitry and/or configuration and all other claims include particular features of circuitry or configuration as to which Schlangenotto is silent, as the Examiner appears to recognize since Schlangenotto has not been applied thereto. Accordingly, reconsideration and withdrawal of the rejections of claims 1 - 6, 8, 35, 36 and 38 is respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

A petition for a two-month extension of time has been made above and the fee therefor submitted by check, which is attached. If any further extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,



Marshall M. Curtis
Reg. No. 33,138

Attachments:
Check for extension of time fee ($200.00)
Check for six excess dependent claims ($54.00)
Copy of originally filed Abstract page

30743
PATENT TRADEMARK OFFICE

APPENDIX

Page 2, line 24+:

Disclosed herein is a family of emitter controlled thyristors (ECT) and emitter turn-off thyristors [(EOT)] (ETO) employing a plurality of control schemes for turning the thyristor on and off. In a first embodiment of the present invention a family of thyristors are disclosed all of which comprise a pair of MOS transistors, the first of which is connected in series with the thyristor (hence after called emitter switch, or Q_E or Q1) and a second which provides a connection from the thyristor gate to the cathode or ground (hence after called gate switch or Q_G or Q2). A third optional MOSFET (hence after called Q_{ON} or Q3) is used to provide the turn-on mechanism for the thyristor. Depending on whether a n-channel or p-channel device is used for Q_E. A negative voltage applied to the gate of the first MOS causes the thyristor to turn on to conduct high currents. A zero to positive voltage applied to the first MOS gate causes the thyristor to turn off. A negative feedback mechanism also exist between the Q_E and Q_G at high currents that causes the ECT to operate at its breakover boundaries of the latching condition with the NPN transistor portion of the thyristor operating in the active region. Under this condition, the anode voltage V_A continues to increase without significant anode current increase. ETO devices disclosed here also use at least two switches Q_G and Q_E to control the current. They also have the negative feedback mechanism that causes the current to saturate at high currents. In particular, ETO fabrication packages are also disclosed having packaged semiconductor devices controlling the thyristor.

Page 6, line 31+:

The ECT can be turned-off by increasing the gate electrode voltage to zero or positive value in PMOS1 10, which interrupts the main current flow path. All currents are then forced to divert to the cathode by the PMOS2 20. Both emitter switch (PMOS1) and emitter short (PMOS2) are used in the turn-off of the ETC., and unlike in the EST, no parasitic thyristor limits the reverse bias [safer] safe operation area (RBSOA) of the [ETC] ECT.

Page 15, line 13+:

Referring now to Figures 7A-B, there is shown a cross-sectional view of the Single Gate NMOS ECT (SNECT) and its equivalent circuit, respectively. The SNECT has a 4-layer PNPN thyristor structure 2 in series with a N channel MOSFET (NMOS 1) 150 integrated on the top of the P well through a Floating Ohmic Contact (FOC) metal strap 152. The FOC 152 connects the upper N+ emitter 154 of the PNPN thyristor and the N + drain region 156 of the NMOS 1. An N-channel depletion mode MOSFET (NMOS2) [158] 162 is also integrated at the surface of the SNECT which acts as the turn-on MOSFET. A P-channel MOSFET (PMOS) 160 is formed between two P regions. The NMOS2 162 and the PMOS 160 share the same gate 164, and the gate is directly tied to the cathode contact 166; hence, the SNECT is a three-terminal device.

Page 16, line 23+:

Referring now to Figures 8A-B, there is shown a cross-sectional view of a single gate emitter controlled thyristor SECT and its circuit equivalent, respectively. The SECT has a 4-layer PNPN thyristor structure 2 in series with a P channel MOSFET (PMOS1) 180 integrated on the surface of the N substrate through a Floating Ohmic Contact (FOC) metal strap 182.

The FOC 182 connects the upper N+ emitter 184 of the PNPN thyristor and the P source region 186 of the PMOS1 180. The FOC 182 provides the bridge for transferring emitter electron currents of the upper NPN transistor into hole currents, which then flow through the PMOS1 180 channel and into the cathode contact. An N-channel depletion mode MOSFET (NMOS) 188 is also integrated at the surface of the SECT which acts as the turn-on MOSFET. A second PMOSFET (PMOS2) 190 is formed between the turn-on NMOS 188 and the PMOS 1 180 with the upper P base acting as its source. The NMOS 188 and the PMOS2 190 share the same gate[196], and the gate is directly tied to the cathode contact [192], hence, the SECT is a three-terminal device.

Claims 1, 19, 34 and 37

1. (Amended) An emitter controlled thyristor device having a cathode terminal and an anode terminal, comprising:

a thyristor device having a thyristor emitter, a thyristor collector, and a thyristor gate, said thyristor comprising alternating P-type and N-type semiconductor regions;

a first metal oxide semiconductor transistor (MOS) connected in series with said thyristor between said cathode terminal said thyristor emitter, said first MOS transistor integrated in at least one of the semiconductor regions of said thyristor; [and]

a second MOS transistor integrated in at least one of said semiconductor regions connected between said cathode terminal and said thyristor gate, a gate terminal of said second MOS transistor connected to said cathode terminal[,]; and

means for shorting said emitter of said thyristor element to a terminal of said first switch or for injecting electrons into said thyristor for triggering said thyristor into said latching state;

wherein a first voltage applied to a gate terminal of said first MOS transistor causes a forward current to flow between said cathode terminal and said anode terminal turning said emitter controlled thyristor device to an on state, and a zero to second voltage turns applied to said gate of said first MOS transistor turns said emitter controlled thyristor device to an off state.

19. (Amended) An gate turn-off (GTO) thyristor device package comprising:

a first metal plate;

a second metal plate;

a third metal plate electrically insulated from said second metal [layer] plate;

a thyristor sandwiched between said first metal plate and said second metal plate, a collector of said thyristor contacting said first metal plate acting as an anode for said [ETO] GTO thyristor device package;

a [first metal oxide semiconductor (MOS) transistor] switch positioned on said second metal plate adjacent said thyristor, said first [MOS transistor] switch having a first terminal connected to an emitter of said thyristor and a second terminal connected to said third metal plate acting as a cathode for said ETO device package; and

a second [MOS transistor] switch positioned on said second metal plate adjacent said thyristor, said second [MOS transistor] switch having a first terminal connected to a gate of said thyristor, said second [MOS transistor] switch further having a second terminal and a gate terminal connected to said third metal plate,

wherein a first voltage applied to a gate terminal of said first MOS transistor turns said thyristor to an on state causing a current to flow between said cathode and said anode, and a zero to second voltage applied to said gate of said first MOS transistor turns said

emitter controlled thyristor device to an off state.

20. (Amended) [An] A gate turn-off (GTO) thyristor device package as recited in claim 19, further comprising a clamp means for holding said first, second and third metal layers together.

21. (Amended) [An] A gate turn-off (GTO) thyristor device package as recited in claim 19, wherein said first, second and third metal plates comprise copper plates.

22. (Amended) [An] A gate turn-off (GTO) thyristor device package as recited in claim [19] 39, wherein said first and second switches are first and second MOS transistors, respectively, and said first MOS transistor and said second MOS transistor are complementary.

23. (Amended) [An] A gate turn-off thyristor (GTO) device package comprising:

a gate turn-off (GTO) thyristor comprising a thyristor gate, a thyristor emitter, and a thyristor collector forming an anode terminal;

a plurality of MOS transistors connected in parallel arranged in a circular fashion around said GTO thyristor, a first terminal of said MOS transistors connected to said thyristor emitter and a second terminal of said MOS transistors connected to a cathode terminal of said GTO device package; and

a plurality of [MOS] switching devices connected in parallel arranged in a circular fashion around said GTO thyristor, a first terminal of said [MOS] switching devices connected to said thyristor gate and a second terminal of said [MOS] switching devices connected to said cathode terminal of said GTO device package,

wherein a first voltage applied to a gate terminal of said MOS transistors turns said GTO thyristor to an

on state causing a current to flow between said cathode terminal and said anode terminal, and a zero to second voltage applied to said gate of said MOS transistors turns said GTO thyristor to an off state.

24. (Amended) [An] A gate turn-off thyristor (GTO) device package as recited in claim 23, further comprising:

a first metal plate forming said cathode terminal;

a second metal plate separated from said first metal plate by an insulation layer, wherein said GTO thyristor and said MOS transistors and said [MOS] switching devices are positioned on said second metal plate, said first and second metal plates acting as a heat sink.

25 (Amended) [An] A gate turn-off thyristor (GTO) device package as recited in claim 23 further comprising a third metal plate [on top of said GTO thyristor] forming and anode terminal of said GTO thyristor device package.

26. (Amended) [An] A gate turn-off thyristor (GTO) device package as recited in claim 23 wherein said [MOS] switching devices comprise a MOSFET transistor having a gate connected to said cathode terminal.

27. (Amended) [An] A gate turn-off thyristor (GTO) device package as recited in claim 23 wherein said [MOS] switching devices comprise a diode.

28. (Amended) [An] A gate turn-off thyristor (GTO) device package as recited in claim 23 wherein said [MOS] switching devices comprise a diode connected in parallel with a capacitor.

29. (Amended) [An] A gate turn-off thyristor (GTO) device package as recited in claim 23 wherein said [MOS] switching devices comprise a Zener diode connected in parallel with a capacitor.

30. (Amended) [An] gate turn-off thyristor (GTO) device package as recited in claim 23 wherein said [MOS] switching devices comprise a transistor connected in parallel with a capacitor.

31. (Amended) [An] A gate turn-off thyristor (GTO) device package as recited in claim 26 further comprising;

a first feedback path connecting said gate terminal of said MOS transistors to said thyristor emitter; and

a second feedback path connecting said gate terminal of said MOS transistors to said thyristor gate terminal through a diode.

33. (Amended) An emitter turn-off thyristor device including

a thyristor device having an anode terminal, a cathode terminal and a gate terminal,

a first semiconductor switch in series with said cathode terminal of said thyristor device by a first terminal of said first semiconductor switch,

as second semiconductor switch in series with said gate terminal of said thyristor device by a first terminal of said second semiconductor switch; second terminals of said first and second semiconductor switches being connected together, and

means for shorting said emitter of said thyristor element to a terminal of said first switch or for injecting electrons into said thyristor for triggering said thyristor into said latching state;

wherein said first and second semiconductor

switches are arranged such that a signal of a first type applied to [control electrodes of] said first and second electronic switches turn said emitter turn-off thyristor to an on-state and a signal of a second type applied to [control electrodes of] said first and second electronic switches turn said emitter turn-off thyristor to an off-state.

34. (Amended) An emitter turn-off thyristor as recited in claim 33, wherein said thyristor device and at [leasat] least one of said first and second semiconductor switches are formed monolithically.

37. (Amended) An emitter turn-off thyristor as recited in claim 33, wherein at least one of said first and second semiconductor [devices] switches is an MOS device.